said selected depth comprising a first layer of the monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a second layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

forming a semiconductor device on said second layer of monocrystalline semiconductor material or on layer of epitaxial monocrystalline semiconductor material deposited on said second layer, and

wherein the said semiconductor device is formed on said epitaxial layer.

---

26. (amended) A semiconductor device formed by the process comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below

said selected depth comprising a first layer of the monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a second layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites;

wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicone ions;

wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide; and

forming a semiconductor device on said bonded substrate.

30. (amended) The substrate of claim 28 wherein said monocrystalline semiconductor material comprises silicon implanted with silicon ions.

38. (new)A bonded semiconductor-on-insulator substrate for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planer intrinsic gettering zone of substantially pure

semiconductor material and active gettering sites positioned between the first and second layers;

a handle wafer; and

an insulating bond layer bonding the handle wafer to the second surface of the wafer.

39. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first and second monocrystalline semiconductor material comprises silicon implanted by silicon ions.

40. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer of monocrystalline semiconductor material.

41. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

42. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

43. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

44. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

45. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

46. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the first layer.

47. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 46, further comprising:

two or more semiconductor devices formed in the epitaxial moncrystalline semiconductor material, wherein the semiconductor devices are laterally isolated from each other.

48. (new) The bonded semiconductor-on-insulator substrate for an integrated circuit of claim 38, further comprising:

two or more semiconductor devices formed in the bonded semiconductor-on-insulator substrate, wherein each semiconductor device is laterally isolated from each other.

49. (new) A bipolar junction transistor for an integrated circuit comprising:

a wafer, the wafer having a first layer of monocrystalline semiconductor material adjacent a first surface of the wafer, the wafer further having a second layer of monocrystalline semiconductor material adjacent a second surface of the wafer, the wafer further having a substantially planer intrinsic gettering zone of substantially pure semiconductor material and active gettering sites positioned between the first and second layers;

a handle wafer;

an insulating bond layer bonding the handle wafer to the second surface of the wafer;

a layer of epitaxial monocrystalline semiconductor material deposited on the first layer;

an emitter diffusion formed in the epitaxial monocyrstalline semiconductor material;

a base diffusion formed in the epitaxial monocyrstalline semiconductor material; and

a collector sinker diffusion formed in the epitaxial monocyrstalline semiconductor material, wherein the emitter, base and collector sinker diffusions are laterally isolated from other devices formed in the epitaxial monocyrstalline semiconductor material of the integrated circuit.

50. (new) The bipolar junction transistor for an integrated circuit of claim 49, wherein the first and second monocrystalline semiconductor material comprises silicon implanted by silicon ions.

51. (new) The bipolar junction transistor for an integrated circuit of claim 49, further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on the second layer of monocrystalline semiconductor material.

B4 cont

52. (new)The bipolar junction transistor for an integrated circuit of claim 49, wherein the handle wafer comprises silicon and the insulating bond layer comprises silicon dioxide.

53. (new) The bipolar junction transistor for an integrated circuit of claim 49, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

54. (new) The bipolar junction transistor for an integrated circuit of claim 49, wherein the second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

55. (new) The bipolar junction transistor for an integrated circuit of claim 49, wherein the gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

B4 Concld

56. (new) The bipolar junction transistor for an integrated circuit of claim 49, wherein the first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

CONCLUSION

Applicant has previously canceled claims 1-23 without prejudice or disclaimer, amended claims 24, 26 and 30 and added new claims 38 - 56 hereby. Claims 24-56 are now pending.

Applicant respectfully requests entry and examination of all pending claims. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2206.

The Commissioner for Patents is hereby authorized to charge any additional fees or credit any overpayments to Deposit Account No. 501373.

Respectfully submitted,

Date: September 4, 2001

Scott V. Lundberg
Reg. No. 41,958

Attorneys for Applicant
Fogg, Slifer & Polglaze, P.A.
P.O. Box 581009
Minneapolis, MN 55458-1009

T – 612/312-2206
F – 612/312-2250